DOUBLE DIFFUSED FIELD EFFECT TRANSISTOR HAVING REDUCED ON-RESISTANCE

Statement of Related Application

[0001] This application is a divisional of co-pending U.S. Patent Application serial number 09/819,356, filed March 28, 2001, entitled "Double Diffused Field Effect Transistor Having Reduced On-Resistance," which is incorporated by reference in its entirety herein.

Field Of The Invention

[0002] This invention relates generally to semiconductor wafer processing and more particularly to a method for forming a double diffused field effect transistor.

Background Information

[0003] Power MOSFET devices are well known and are used in many applications including automotive electronics, portable electronics, power supplies, and telecommunications. One important electrical characteristic of a power MOSFET device is its on-state resistance (R_{DSon}), which is defined as the total resistance encountered by the carriers as they flow from the source terminal to the drain terminal. In order to allow manufacturers to produce power MOSFET devices having higher current carrying capability in smaller packages, it would be advantageous to have MOSFET structures that reduce the on-state resistance

[0004] FIG. 1 is a simplified cross-sectional diagram of a conventional n-channel power MOSFET referred to as a double diffused field effect transistor. A layer of N type epitaxial silicon 1 is formed on an N+ type substrate 2. A P body region 3A and a P+ body region 3B are formed into the epitaxial layer from upper surface 4, and an N+ type source region 5 is formed into the body regions 3A and 3B from upper surface 4. To turn the transistor on (i.e., make it conductive), a positive potential is placed on gate 6. The positive potential on gate 6 causes what is called a channel region to form in the surface portion of P body region 3A underneath the gate and also causes what is called an accumulation region to form in the surface portion of the N type epitaxial silicon region